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Cache index = n if 2^n = number of blocks

Task 1:

Num Blocks = 8

Cache block size = 4 words

Cache size = 128 bytes

1. Number of bits for the default cache configuration
   1. Block offset – +4
   2. Cache index – 3
   3. Tag – 0x200200
2. Assemble the program and set a breakpoint at the instruction right after lw. Write down the address of the instruction as we will use it often.
   1. Instruction address – 0x10010000

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Address | Cache Index | Tag | Block Offset | Hit/Miss |
| 0x10010000 | 0 | 0x00200200 | 0 | Miss |
| 0x10010004 | 0 | 0x00200200 | 4 | Hit |
| 0x10010008 | 0 | 0x00200200 | 8 | Hit |
| 0x1001000c | 0 | 0x00200200 | 12 | Hit |
| 0x10010010 | 1 | 0x00200200 | 0 | Miss |
| 0x10010014 | 1 | 0x00200200 | 4 | Hit |

1. Explanation of the cache index, tag and block offset for the first 2 accesses.
   1. The cache index of the first 2 interactions is 0 since we are in the first cache block.
   2. The tag for the first two interactions is the same and they stay the same but this is because we do not move very far in the cache block and this is the initial tag.
   3. The block offset for the first interactions is 0 since we are at the start and then it is 4 since we move by a factor of n if 2^n = number of bytes in the words of the cache. So n is 4.
2. Explanation of the hit/miss outcomes for each table entry. (Table should have 6 entries)

The miss at the start of the table is because nothing is in the cache yet. Then we have 3 hits since we are in are because we are referencing the same register and still in the first cache index. The second miss is because we have moved to the second cache index so it is like resetting but then we get another hit since the register is now loaded into this part of the cache also.

1. Explanation of observed cache hit rate

The observed cache hit rate is 75 since for every 4 time we check the cache we get 1 miss and 3 hits. ¾ = .75 or 75%.

Task 2

Block size = 4 words

Num blocks and Cache size varies

1. Table

|  |  |  |  |
| --- | --- | --- | --- |
| Number of Blocks | Cache Size | Hit Rate | Miss Count |
| 8 | 128 Bytes | 75% | 3072 |
| 16 | 256 | 75% | 3072 |
| 32 | 512 | 75% | 3072 |
| 64 | 1024 | 99% | 64 |
| 128 | 2048 | 99% | 64 |

1. Explanation of cache hit/miss rate

The cache hit rate starts at 75% but increases once our cache gets bigger.

1. If size of warray is doubled, which rows in the table will change, explain.

The only cell in the table that would change would be the “Hit Rate” for the number of blocks 64 since we would not have enough cache to cover the entire array yet but when we increased the cache one more time we would.